A. Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) An integrated circuit comprising:

a plurality of functional modules formed within said integrated circuit interconnected via a packet router formed within said integrated circuit, each functional module having packet handling circuitry for generating and receiving packets conveyed by the packet router;

wherein at least a first set of said functional modules, acting as initiator modules, have packet handling circuitry which includes request packet generation circuitry for generating request packets for implementing transactions, each request packet including a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes the type of the packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function, and

wherein a second set of the functional modules, acting as target modules, each have packet handling circuitry which includes packet receiver logic for receiving said request packets and for generating respective response packets, wherein the single packet type bit distinguishes between request packets and response packets.

2. (Cancelled).

3. (Previously Presented) An integrated circuit according to claim 1, wherein the function in each request packet is a memory access operation.

4. (Original) An integrated circuit according to claim 3, wherein one of said operation family bits distinguishes between primitive memory access operations involving a single request packet and compound memory access operations involving a plurality of request packets.

5. (Original) An integrated circuit according to claim 1, wherein each request packet includes a data object, the size of which is denoted by the three bit operation qualifier.

6. (Previously Presented) An integrated circuit comprising:

a plurality of functional modules formed in said integrated circuit and interconnected via a packet router formed in said integrated circuit, each functional module having packet handling circuitry for generating and receiving packets conveyed by the packet router;

wherein at least a first set of said functional modules acting as initiator modules, have packet handling circuitry which includes request packet generation circuitry for generating request packets for implementing transactions, each request packet including a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes the type of the packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function, and

wherein a second set of said functional modules, acting as target modules, each having packet handling circuitry which includes packet receiver logic for receiving said request packets and for generating respective response packets, wherein the single packet type bit distinguishes request packets and response packets.

7. (Previously Presented) An integrated circuit comprising:

a plurality of functional modules formed in said integrated circuit and interconnected via a packet router formed in said integrated circuit, each functional module having packet handling circuitry for generating and receiving packets conveyed by the packet router;

wherein each functional module has packet handling circuitry which includes request packet generation circuitry for generating request packets for implementing transactions, and packet receiver logic for receiving request

packets and for generating respective response packets, each request packet including a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the packet, wherein the operation field comprises eight bits of which a single packet type bit distinguishes between request packets and response packets, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function.

8. (Original) An integrated circuit according to claim 7, wherein each request packet includes a data object, the size of which is denoted by the three bit operation qualifier.

9. (Previously Presented) An initiator functional module for connection in an integrated circuit comprising:

an interface for supplying and receiving packets to and from the functional module, said interface being connected to a port for connecting the functional module to a packet router, wherein both the initiator functional module and the packet router are formed within the integrated circuit;

packet handling circuitry for handling said packets and including request packet generating logic which generates request packets for supply to the packet router via the interface, each request packet having a destination indicator identifying a destination of the packet and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes a request or response packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function.

10. (Previously Presented) A target functional module for connection in an integrated circuit comprising:

an interface for supplying and receiving packets to and from the functional module, said interface being connected to a port for connecting a functional

module to a packet router, wherein both the target functional module and the packet router are formed within the integrated circuit;

packet receiver logic which is operable to receive request packets supplied from the packet router via the interface to the target functional module, each request packet having an operation field denoting the function to be implemented by the request packet, said operation field including four operation family bits denoting the function to be implemented by the packet, one of said operation family bits distinguishing between primitive memory access operations and complex memory access operations, wherein the packet receiver logic comprises means for detecting the status of said one operation family bit to determine whether the memory access operation is primitive or compound; and

means for generating respective response packets on receipt of each request packet, wherein the operation field of both request and response packets includes a single packet type bit which distinguishes between request packets and response packets.

11. (Cancelled)

12. (Previously Presented) A method of implementing transactions in an integrated circuit comprising a plurality of functional modules interconnected via a packet router, the method comprising:

at one of said functional modules acting as an initiator module within said integrated circuit, generating a request packet including a destination indicator identifying a destination of the packet within said integrated circuit and an operation field denoting the function to be implemented by the request packet, wherein the operation field comprises eight bits of which a single packet type bit denotes the type of a packet, four operation family bits denote the function to be implemented by the packet and three operation qualifier bits act to qualify the function;

at the destination indicated by the destination indicator, receiving said request packet and identifying the function to be implemented from the four operation family bits and the operation qualifier bits; and

generating a response packet for transmission to the initiator functional module, wherein the single packet type bit distinguishes between request packets and response packets.

13. (Original) A method according to claim 12, wherein the function in each request packet is a memory access operation.

14. (Original) A method according to claim 13, wherein one of said operation family bits distinguishes between primitive memory access operations involving a single request packet and compound memory access operations involving a plurality of request packets, and wherein the method comprises detecting at the destination of the packet the status of this bit to determine whether a primitive memory access operation or a compound memory access operation is to be implemented.

15. (Original) A method according to claim 12, wherein each request packet includes a data object, the size of which is denoted by the three bit operation qualifier, the method comprising at the destination of the packet, detecting the size of said data object from the three bit operation qualifier to determine how to implement the function in the request packet.

16. (Original) A method according to claim 13, wherein said memory access operations include load, store, read-modify-write and swap operations.

17. (Original) An integrated circuit according to claim 3, wherein the memory access operation includes cache operations.

18. (Original) An integrated circuit according to claim 1, wherein the four operation family bits denote that the operation field is user defined.

19. (Original) A method according to claim 13, wherein said memory access operation includes cache operations.

20. (Original) A method according to claim 12, wherein said four operation family bits denote that the function defined in the operation field is user defined.